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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/943,586	08/30/2001	Neal Andrew Crook	MIC-13	9394

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EXAMINER	
PAN, DANIEL H	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 11/05/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/943,586	CROOK ET AL.	
	Examiner	Art Unit	
	Daniel Pan	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 August 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,7-10,12-14,16-19,21-24,26-28 and 31-36* is/are rejected.

7)☒ Claim(s) *6,11,15,20,25,29 and 30* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 August 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. Claims 1-36 are presented for examination.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-4, 7,8,10, 12-14, 16, 17-19, 21,22, 33-35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gazdik (6,324,691) in view of Yamaguchi (6,110,229) .

3. As to claims 1,2, 7, 10, 12-14, 17, 18,32, 33-35 Gazdik disclosed a system including at least :

a) receiving a program code , data and control information form data path (see the input path of computer system 14 from install engine in fig.1);

b) reading identifying information for indicating the program data [software components] (see identification of the software components in col.6, lines 15-20);

c) processing setup received in the data path (see the PC COMmnad and Pinstall Objects for performing installations of the software components in col.6, lines 53-67, col.7, lines 1-57, see also the persistent data file 13 including information required for install and copied into distributed medium in computer system 14 in col.5, lines 5-24 for background);

d) process program data received in the input path accordance with the identification information (see the software components to provide services and functionalities in the computer system in col.6, lines 15-30, lines 53-57).

e) switching from setup to run mode (see the switch to run installation program in col.8, lines 35-46).

4. Gazdik did not specifically show his identification information was a identification bit to indicate one of the setup data and program data (claims 1,12, 32), nor determination of the received information was setup or program data (claims 17, 35) as claimed . Instead, it only showed identification information for indicating the program data [software components] (see col.6, lines 15-20. However, Yamaguchi disclosed a system including identification information bit for selecting a setup environment (see the D bit for selecting the setup in col.5, lines 9-14, see also the setup format as one of the environment elements in col.4, lines 65-67, col.5, lines 1-8). It would have been obvious to one of ordinary skill in the art to use Yamaguchi in Gazdik for including the identification bit for indicating one of the setup and program data , or to determining whether the setup or program data was received as claimed because the use of Yamaguchi could provide control capability of Gazdik to adapt to the selection of the setup and program data in a predefined integrated format, such as an identification bit for determination the type of information , thereby minimizing the use of hardware overheads, and it could be readily achieved by defining the information bit of Yamaguchi into the identification information of Gazdik with modified control attributes (e.g. the bit length, and bit type) so that the identification bit of Yamaguchi could be recognized

by Gazdik in order to provided the enhanced integrated format of the identification information, and for the above reasons, provided a motivation.

5. As to claim 3, Gazdik was also directed to setup data (see the install information in col.2, lines 34-67).

6. As to claim 4, Gazdik was also directed to a storage medium, such as a memory (see fig.1).

7. As to claims 8, as the fetching , decoding and storing the result from executing instructions , the examiner holds that all these operations had been standard operations in the art. No specific detail or format of the fetch g, decoding ,the storage , has been reflected into the claim, therefore, it is treated as general fetching, decode and storage operation.

8. As to the feature of automatically switching from run mode to install mode in claim 12, Gazdik showed the setup mode to run mode (see the switch to run installation program in col.8, lines 35-46). However, it did not explicitly show the switching g form rum mode to setup mode as claimed. However, Gazdik , in the same patent., taught the elimination of the need for user interaction to perform several download the setup program [installation program] will install software without requiring user's interaction (se col.2, lines 12-33). Therefore, it is for this reason, the examiner believes that the automatic switch of the run mode (e.g. after completion of current software) to setup mode (a next setup) was also applicable in the system.

9. As to claim 16, Gazdik also taught h waiting of the data (e.g. see the priority command in col.7, lines 44-57).

10. AS to claim 19, Gazdik also included input data path (see the input connection in fig.1).

11. As to claim 21, see the program identification bit in Yamaguchi (see the D bit for selecting the setup in col.5, lines 9-14, see also the setup format as one of the environment elements in col.4, lines 65-67, col.5, lines 1-8).

12. AS to claim 22, see discussions and reasons for obviousness in paragraph # above.

13. Claims 5 ,9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gazdik (6,324,691) in view of Yamaguchi (6,110,229) as applied to claims 1, 8 above, and further in view of Dewey et al. (5,652,887).

14. As to claims 5,9, neither Gazdik nor Yamaguchi specifically showed the increment of the memory address for storing the instructions as claimed. However, Dewey disclosed a system for storing instruction in a buffer at an increment of address size (e.g. see the increment pointer in col.7, lines 1-17). It would have been obvious to one of ordinary skill in the art o use Dewey in Gazdik for incrementing address as claimed because the use of Dewey could provide the storage of the software components of Gazdik in a predefined set of sequence, such as the incremented address segment, therefore, enhancing the storage format of Gazdik, and because Gazdik did disclose a storage of his program components into a storage medium (see fig.1), and therefore, it would have been recognizable by one of ordinary skill in the art

that the use of address increment was applicable into the storage medium for access purpose, such as the read and write.

15. Claims 23, 24,26-28,31, 32,36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pickett (5,968,169) in view of Gazdik (6,324,691) .

16. As to claims 23, 24,26,31, 36, Pickett disclose at least :

a) execution pipeline including a first input and second input (e.g. see the input and output connections to [ALU's] in fig.5, see also col.1, lines 15-25 for the background teaching of pipeline execution, see also col.19, lines 56-63);

b) a memory [502] comprising a first input coupled to the pipeline execution (see fig.1 the feedback path from functional unit [212] to instruction cache 204 through prediction unit [220]) and second input (see fig.5 [502]);

c) program counter comprising input and output coupled to the memory (see fig.5, pc counter not explicitly shown, see the counter in col.23, lines 3-14);

d) control logic (see the instruction alignment unit , decode unit, the operand steering unit , operand and result buses and all output connections in ALU's in fig.5) comprising :

1) first input coupled to the execution pipeline output (see the output connection of result bus to input of steering unit);

2) second input coupled to the output (see the output to the input of alignment unit);

3) third input coupled to the output of program counter (not explicitly shown , but see the prefetch buffer counter in fig.17 and the predictor counter in fig.20);

4) first output coupled to the program counter input (see the input to the prefetching and branch predictor in fig.5) ;

e) a register file [register file 518] comprising a first input to the output of the execution pipeline (see result buses to register file 518 through buffer 516 in fig.5);

f) second input to second output of control logic (see output from register file 518 to input of the operand steering unit in fig.5);

g) output to second input of the execution pipe (see the output from register file 518 to the ALU's through operand buses in fig.5).

17. Pickett did not specifically show the receipt or transfer of the setup data and program data as clamed. However, Gazdik showed the transfer of the setup data and program data (see the PC COMmnad and Pinstall Objects for performing installations or setup of the software components [program data] in col.6, lines 53-67, col.7, lines 1-57, see also the persistent data file 13 including information required for install and copied into distributed medium in computer system 14 in col.5, lines 5-24 for background). It would have been obvious to one of ordinary skill in the art o use Gazdik in Pickett for including the setup and program data as claimed because the use of Gazdik could provide Pickett the ability of the microprocessor to adapt to new configuration requirements from external resources, such as new version of program components or data in a host, therefore enhancing the compatibility of the system, and because no specific format of the setup and program data ahs been reflected into the claim, the setup and program data are being treated as any general information used for executing the program in a given computer system, and therefore, one of ordinary

skill in the art should be able to recognize the advantages of the transferring setup and program data into any system, such as the one taught by Pickett in order to achieved the enhanced adaptability, and for the above reasons provided a motivation.

18. As to claims 27-28, Pickett also included counter for memory address (see the pc address values in col.46, lines 31-67).

As to claim 32, Pickett' register file was also used for receive the result data form the execution pipeline (see result buses to register file in fig.5).

19. Claim 6 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. None of the prior art of record further teaches the increment of the register file counter for second constant in addition to the loading of the constant at the loading value.

20. Claim 11 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. None of the prior art of record further teaches the generation of output data identification signals to allow the input value being interleaved with the data.

21. Claims 15,20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. None of the prior art of record further

teaches the switching go the run mode to setup mode by executing the pass through instruction that causes the setup data to propagate to execution pipe without modification.

22. Claim 25 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. None of the prior art of record further teaches the pass through instruction when the data from input path was a setup data, propagated through without modification.

23. Claim 29 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. None of the prior art of record further teaches the write memory address when the data was a setup data and the e read memory address when the data was a program data.

24. Claim 30 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. None of the prior art of record further teaches the fourth input of the control logic to receive the identification bit to indicate whether the data was setup data or program data.

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a) Lin (5,689,726) is cited for the teaching of the automatic loading of te seup data into a memory (e.g see col.8, lines 29-64).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dan Pan whose telephone number is 703 305 9696, or the new number 571 272 4172. The examiner can normally be reached on M-F from 8:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chan, can be reached on 703 305 9712, or the new number 571 272 4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

21 Century Strategic Plan

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